A Method f r Making Nan scale Wires and Gaps f r Switches and Transistors

Field of the Invention

The present invention relates to nanoscale electric devices, and more particularly, to a method for making nanoscale wires and gaps for switches and transistors.

Background of the Invention

Reducing the feature size of integrated circuit components is a continuing goal of semiconductor process designers. In the past, such reductions have led to decreased cost and increased operating speed. Device fabrication depends on techniques that rely on masks to define the boundaries of the transistors and conductors. For example, metal and semiconductor conductor patterns are fabricated by lithography in which masks determine the location and size of the patterns. The conductivity in semiconductors can also be controlled by implanting ions. The areas that are to be implanted are typically defined by an opening in a mask. Similarly, transistors require the selective implantation of ions. Unfortunately, conventional masking techniques are inadequate when nanometer scale components are to be fabricated.

Broadly, it is the object of the present invention to provide a self-assembled masking technique for use in fabricating nanoscale wires and devices in integrated circuits.

These and other objects of the present invention will become apparent to those skilled in the art from the following detailed description of the invention and the accompanying drawings.

Summary of the Invention

The present invention is a method for forming first and second linear structures of a first composition that meet at right angles, there being a gap at the point at which the structures meet. The linear structures are constructed on an etchable crystalline layer having

the first composition. First and second self-aligned nanowires of a second composition are grown on a surface of the etchable crystalline layer, the first nanowire growing at right angles to the second nanowire. The first nanowire is separated from the second nanowire by a gap of less than 10 nm at their closest point. Portions of the etchable layer that are not under the first and second nanowires are then etched using the first and second nanowires as a mask thereby forming the first and second linear structures of the first composition. The nanowires are grown by depositing a material of the second composition which forms crystals on the surface that have an asymmetric lattice mismatch with respect to the crystalline surface. The linear structures so formed are well suited for the fabrication of nanoscale transistors having a first elongated doped semiconductor wire having a width between 1-100 nm on an insulative substrate. A second wire at right angles to the first ridge acts as the gate of the transistor. The two wires are separated by a gap of between 0.4 and 10 nm at their closest point. By filling the gaps with appropriate materials, the wires and gaps can also function as a nanoscale memory switch and a transistor.

Brief Description of the Drawings

Figures 1(A)-(C) are prospective views at various stages in the fabrication process of a substrate 12 in which nanowires are to be constructed.

Figure 2 is a top view of a portion of a substrate 20 on which two self-assembled nanowires and a nanoscale gap shown at 21 and 22 have been grown.

Figure 3 is a perspective view of a semiconductor nanowire structure that forms a transistor.

Detailed Description of the Invention

The present invention is based on the observation that thin "nanowires" of $ErSi_2$ can be grown epitaxially on the (001) plane of silicon without masking the silicon. The manner in which these wires are grown is discussed in detail in "Self-assembled growth of epitaxial erbium disilicide nanowires on silicon (001)" by Yong Chen, Douglas A. A. Ohlberg,

Gilberto Medeiros-Ribeiro, Y. Austin Chang, and R. Stanley Williams in **Applied Physics Letters, 76**, p. 4004, June 2000, which is hereby incorporated by reference. The $ErSi_2$ nanowires are grown by depositing Er on the surface of the silicon and then heating the silicon to drive the reaction to completion. The Er can be deposited with an *in situ* electron-beam evaporator at temperatures between room temperature and 620°C. The annealing operation can be carried out at temperatures between 575 and 800°C. The resulting nanowires are oriented along the two perpendicular <110> directions ([110] and [1-10]) and at right angles thereto.

The self-assembly of the nanowires depends on an asymmetric lattice mismatch between the ErSi2 and the underlying silicon substrate. The overlayer material must be closely-lattice matched to the substrate along one major crystallographic axis but have a significant lattice mismatch along all other crystallographic axes within the interface between the epitaxial crystal and the substrate. In principle, this allows the unrestricted growth of the epitaxial crystal in the first direction but limits the width in the other.

While the example given herein utilizes $ErSi_2$ grown over Si, other materials and substrates can be utilized. In general, any crystalline material that can be characterized by an asymmetric lattice mismatch, in which the first material has a close lattice match (in any direction) with the second material and has a large lattice mismatch along all other crystallographic axes within the interface between the epitaxial crystal and the substrate. For example, $ScSi_2$, $GdSi_2$, and $DySi_2$ grown on Si(001) substrates may also be utilized. Such structures are taught in Yong Chen, Douglas A. A. Ohlberg, and R. Stanley Williams in **Journal of Applied Physics, 91**, p. 3213, March 2002, which is hereby incorporated by reference. A close lattice match means that the absolute value of lattice mismatch between the two crystal materials is less than 4%. A large lattice mismatch means that the absolute value of lattice mismatch between the two crystal materials is within the range of about 4 to 10%. While any crystallographic direction may be chosen, the present invention preferably utilizes a material having the asymmetric lattice mismatch along a major (or low Miller-index) crystallographic direction within the interface between the epitaxial crystal and the substrate. By "major crystallographic direction" is meant any direction along which the crystalline material comprising the nanowire may prefer to grow within the interfacial plane.

In the case of $ErSi_2$, $ScSi_2$, $GdSi_2$, and $DySi_2$ nanowires, the nanowires are typically 2-20 nm wide and have lengths of a few hundred nm. The nanowires are self-elongating once the silicide crystal has been seeded at a particular location. The nanowires can be seeded at locations where special seeding materials or growth windows are predefined by lithography methods.

The manner in which these nanowires are utilized to generate two silicon nanowires at the right angle and a nanoscale gap between them will now be explained with reference to Figures 1(A)-(C) which are prospective views of a silicon substrate 12 in which a single conducting silicon nanowire is to be constructed at various stages in the fabrication process. The upper region 13 of silicon substrate 12 is doped with a suitable element to render the material conducting. An insulating layer 19 such as SiO_x is buried under the conductive layer. The insulating layer typically has a thickness between 1-500 nm. The insulating layer can be made by implanting oxygen ions into the silicon substrate and then annealing the substrate to form a buried layer of SiO_x. An $ErSi_2$ nanowire 14 is then deposited over the region of substrate 12 that is to contain the silicon nanowire. FIG. 1(B) illustrates a prospective view of the present invention wherein the portions of the material that were above the insulating layer but not masked by the nanowire have been removed leaving a ridge 16 having an $ErSi_2$ layer on the top thereof. These portions can be removed by reactive ion etching (RIE). The etching can be stopped at the exposed surface of the insulating layer. Finally, the $ErSi_2$ can be removed, if desired, by selective chemical etching leaving the Si nanowire 18 as shown in Figure 1(C).

The present invention is based on the observation that the $ErSi_2$ nanowires provide a masking pattern that is ideal for the fabrication of nanoscale gaps for transistors and memory switches. The $ErSi_2$ nanowires grow along the [110] crystal direction and also along the [1-10] direction. When two of these nanowires are seeded such that the two nanowires will meet at right angles, a nanoscale gap can be formed between the first and the second nanowires at the point at which one nanowire meets the other nanowire at a right angle. The growth of the first nanowire will be stopped as it gets close to the second nanowire since the two nanowires have different crystallographic orientations.

Refer now to Figure 2, which is a top view of a portion of a silicon substrate 20 on which two $ErSi_2$ nanowires shown at 21 and 22 have been grown. When two $ErSi_2$ wires meet at right angles, a small gap 23 remains between the $ErSi_2$ nanowires. The gap is typically 0.4-10 nm.

Refer now to Figure 3, which is a perspective view of a silicon nanowire structure that forms a switch or a transistor. Transistor 30 is constructed from two silicon nanowires shown at 32 and 33. Nanowire 33 acts as the gate of transistor 30. The ends of nanowire 32 form the source and drain of transistor 30. Nanowires 32 and 33 are fabricated using a mask of the type shown in Figure 2. Due to the small gap distance 34, when a voltage is applied on nanowire 32, the electric field will influence and control the current flow in nanowire 33. The gap can be filled with a material such as molecules, ferroelectric materials, and nanoscale particles that store charge or electric dipole moment in the gap. Hence, the transistor can provide gain or nonvolatile switching for logic and memory applications. If two-electrode devices are formed between the nanowires 32 and 33, an electric field applied between the two electrodes can switch the electric conductivity of the materials adjacent to the gap. Such a device is taught in US Patent 6,128,214, which describes how a memory cell can be formed between the two nanowires.

While the above embodiments of the present invention have been described in terms of masks generated from $ErSi_2$ nanowires, as noted above, other materials can be utilized. In general, any material that has a sufficiently asymmetric lattice mismatch can be utilized over an appropriate substrate. Metal silicides represented as the chemical formula MSi_2 grown over silicon are examples of such nanowire systems. Here, M is a metal selected from the group consisting of Sc, Y, and the rare earths. The preferred rare earths are Er, Dy, Gd, Th, Ho, Tb, Y, Sc, Tm, and Sm.

In principle, any single crystal material that is useful in the fabrication of nanowires may be used in combination with any single crystal material that serves as a layer on which the nanowires can be grown, provided that the asymmetric lattice mismatch conditions

described above are met. The present invention may be practiced using self-assembled crystals grown on single crystal layers such as metals, insulators such as sapphire, and semiconductors such as germanium, III-V compound semiconductors, whether binary (e.g., GaAs, InP, etc.), ternary (e.g., InGaAs), or higher (e.g., InGaAsP), II-VI compound semiconductors, and IV-VI compound semiconductors. Examples of such combinations are listed in U.S. Patent 5,045,408, entitled "Thermodynamically Stabilized Conductor/Compound Semiconductor Interfaces", issued on September 3, 1991, to R. Stanley Williams *et al*, the contents of which are incorporated herein by reference. Specific examples of semiconductor substrate materials include Si, Ge, Ge_xSi_{1-x} where $0 < x < 1$, GaAs, InAs, AlGaAs, InGaAs, AlGaAs, GaN, InN, AlN, AlGaN, and InGaN. Specific examples of metal substrate materials include Al, Cu, Ti, Cr, Fe, Co, Ni, Zn, Ga, Nb, Mo, Pd, Ag, In, Ta, W, Re, Os, Ir, Pt, and Au, and alloys thereof.

Various modifications to the present invention will become apparent to those skilled in the art from the foregoing description and accompanying drawings. Accordingly, the present invention is to be limited solely by the scope of the following claims.